

Application/Control Number: 10/803,592

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IN THE CLAIMS

1. (Currently amended) A semiconductor memory device with a capacitor on a bit line (CBL) cell structure, comprising:

a semiconductor substrate including an isolation region that defines an active area with a plurality of source-drain regions;

a contact pad layer formed on the semiconductor substrate, said contact pad layer including gate line structures, first contact pads connected to parts of the source-drain regions, second contact pads connected to the other source-drain regions, and a first interlevel dielectric layer formed to cover covering the gate line structures and formed to laterally surround the first and second contact pads;

a bit line contact plug layer on the contact pad layer, said bit line contact plug layer including lower storage node contact plugs connected to the first contact pads, bit line contact plugs connected to the second contact pads, a protective layer pattern that covers at least a portion of the second contact pads to prevent the second contact pads from being connected to contacting the lower storage node contact plugs and/or upper storage node contact plugs, and a second interlevel dielectric layer formed to laterally surround the lower storage node contact plugs, the bit line contact plugs, and the protective layer pattern covering the lower storage node contact plugs and the protective layer pattern, and

a bit line layer formed on the bit line contact plug layer, said bit line layer including the upper storage node contact plugs connected to the lower storage node contact plugs, bit line structures connected to the bit line contact plugs, and a third interlevel dielectric layer formed to laterally surround and cover the upper storage node contact plugs and formed to laterally surround and cover the bit line structures.

2. (Original) The semiconductor memory device of claim 1, wherein the protective layer pattern is formed of a material having a high etching selectivity with respect to the second interlevel dielectric layer.

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4 (Original) A semiconductor memory device of claim 2, wherein the second interlevel dielectric layer is formed of a silicon oxide and the protective layer pattern is formed of silicon nitride.

4 (Original) The semiconductor memory device of claim 1, further comprising a capacitor formed on the bit line layer and connected to the upper storage node contact plugs.

5 (Currently Amended) A semiconductor memory device of a COB cell structure in which a plurality of source/drain regions are arranged in a substantially straight line in the length and width directions, the semiconductor memory device comprising:

a semiconductor substrate having a plurality of source/drain regions defined by an isolation region;

a contact pad layer on the semiconductor substrate, the contact pad layer including gate line structures, first contact pads connected to parts of the source/drain regions, second contact pads connected to the other source/drain regions, and a first interlevel dielectric layer formed to cover/covering the gate line structures and formed to laterally surround the first and second contact pads;

a bit line contact plug layer on the bit line contact plug layer, the bit line contact plug layer including lower storage node contact plugs connected to the first contact pads, bit line contact plugs connected to the first contact pads, a protective layer pattern formed on at least a portion of the second contact pads to prevent the second contact pads from being connected to contacting the lower storage node contact plugs and/or upper storage node contact plugs, and a second interlevel dielectric layer formed to laterally surround the lower storage node contact plugs, the bit line contact plugs, and the protective layer pattern covering the lower storage node contact plugs and the protective layer pattern; and

a bit line layer on the bit line contact plug layer, said bit line layer including the upper storage node contact plugs connected to the lower storage node contact plugs and arranged in a zigzag pattern, bit line structures connected to the bit line contact plugs, and a third interlevel dielectric layer formed to laterally surround covering the upper storage node contact plugs and formed to laterally surround and cover the bit line structures.

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6. (Original) The semiconductor memory device of claim 5, wherein the protective layer pattern is formed of a material having a high etching selectivity with respect to the second inter-level dielectric layer.

7. (Original) The semiconductor memory device of claim 6, wherein the second inter-level dielectric layer is formed of silicon oxide and the protective layer pattern is formed of silicon nitride.

8. (Original) The semiconductor memory device of claim 5, further comprising a capacitor on the bit line layer and connected to the upper storage node contact plugs.

9. (Original) The semiconductor memory device of claim 8, wherein lower electrodes of the capacitor are arranged in a zigzag pattern.

10. (Original) The semiconductor memory device of claim 9, wherein lower electrodes of the capacitor are cylinder shaped.